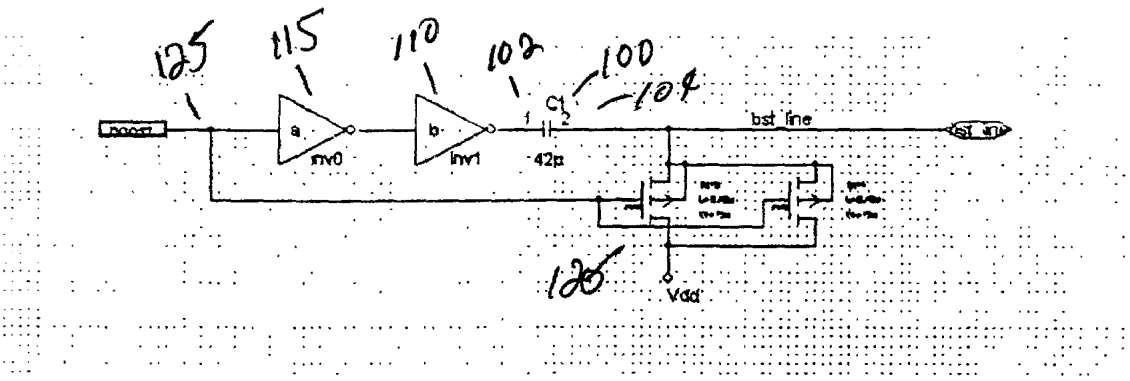

Figure 1. Bootstrap circuit used in our current design

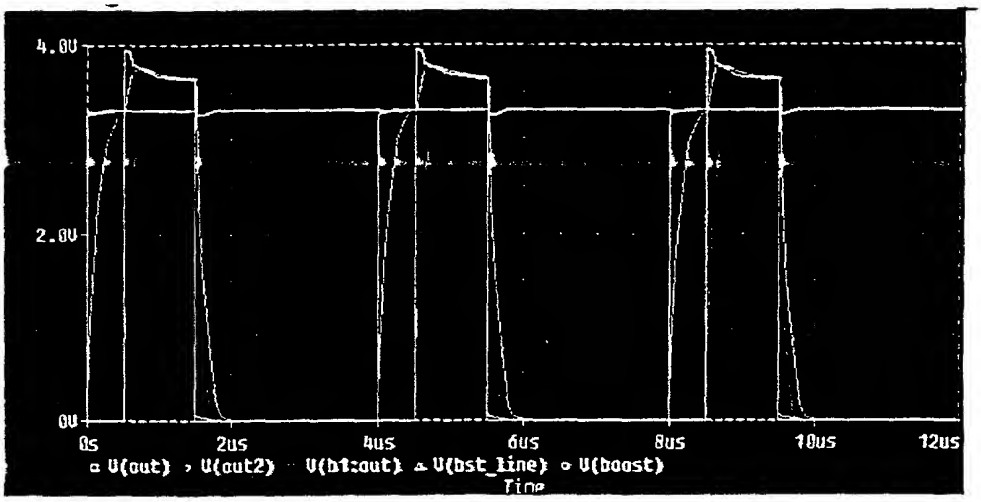

Figure 2. Simulation results from current bootstrap circuit

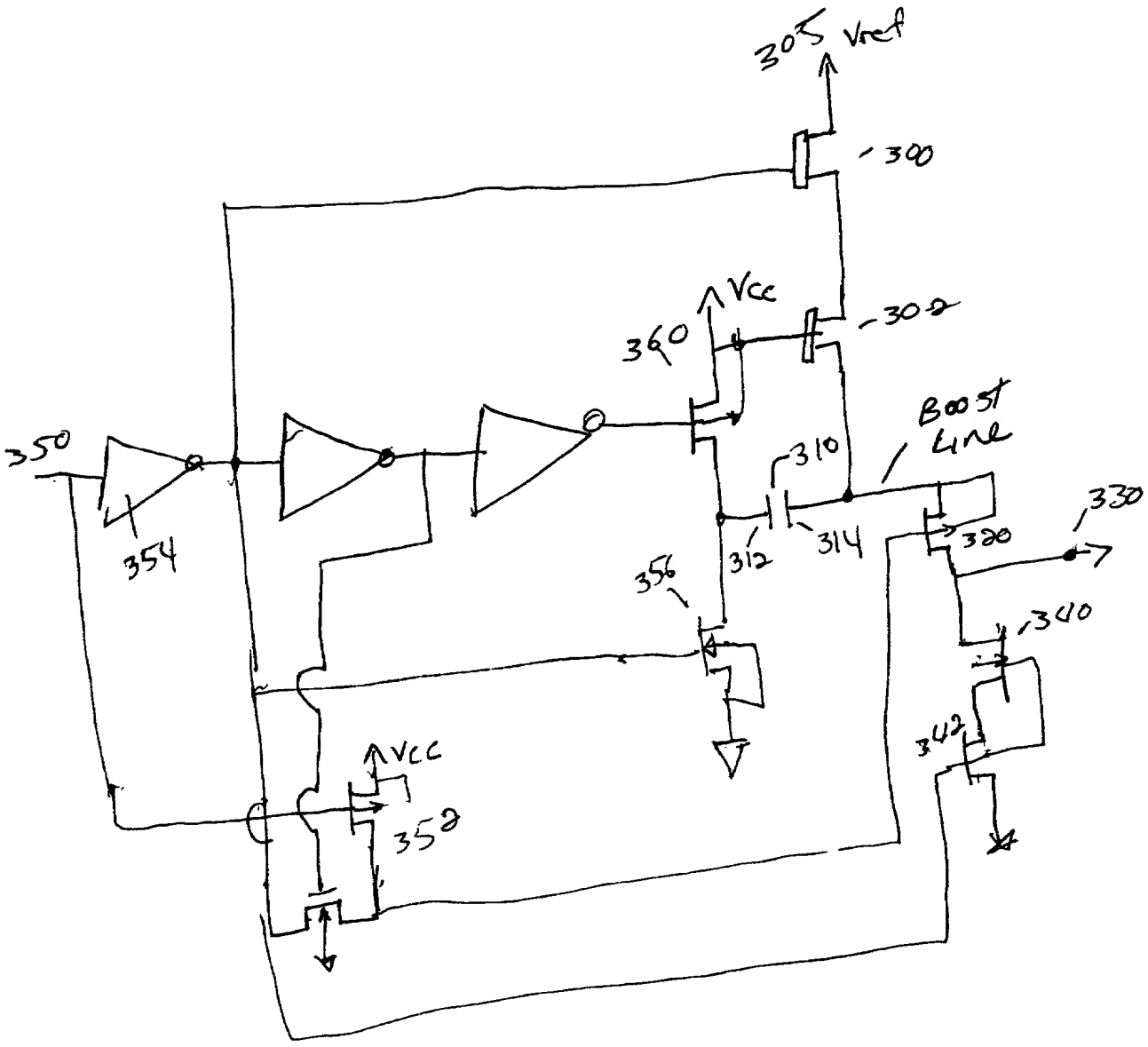
305
Vref
300
Vcc
360
302
350
Boost Line
310
354
312
314
330
320
356
340
342
Vcc
352

FIG 3

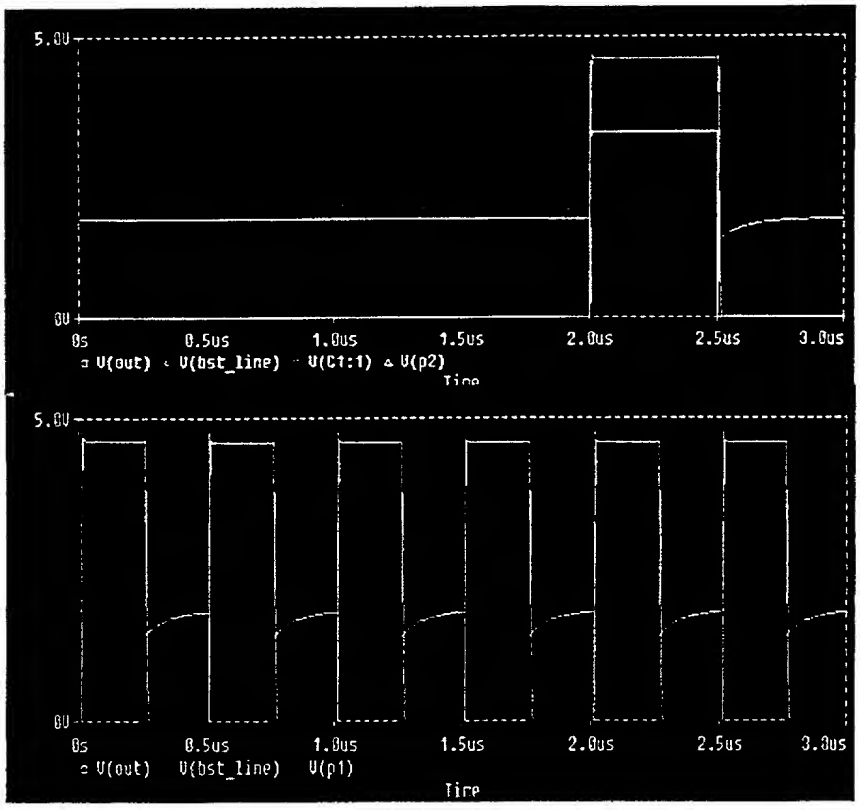

Figure 4. Simulation for single and continuous clock boosting signals

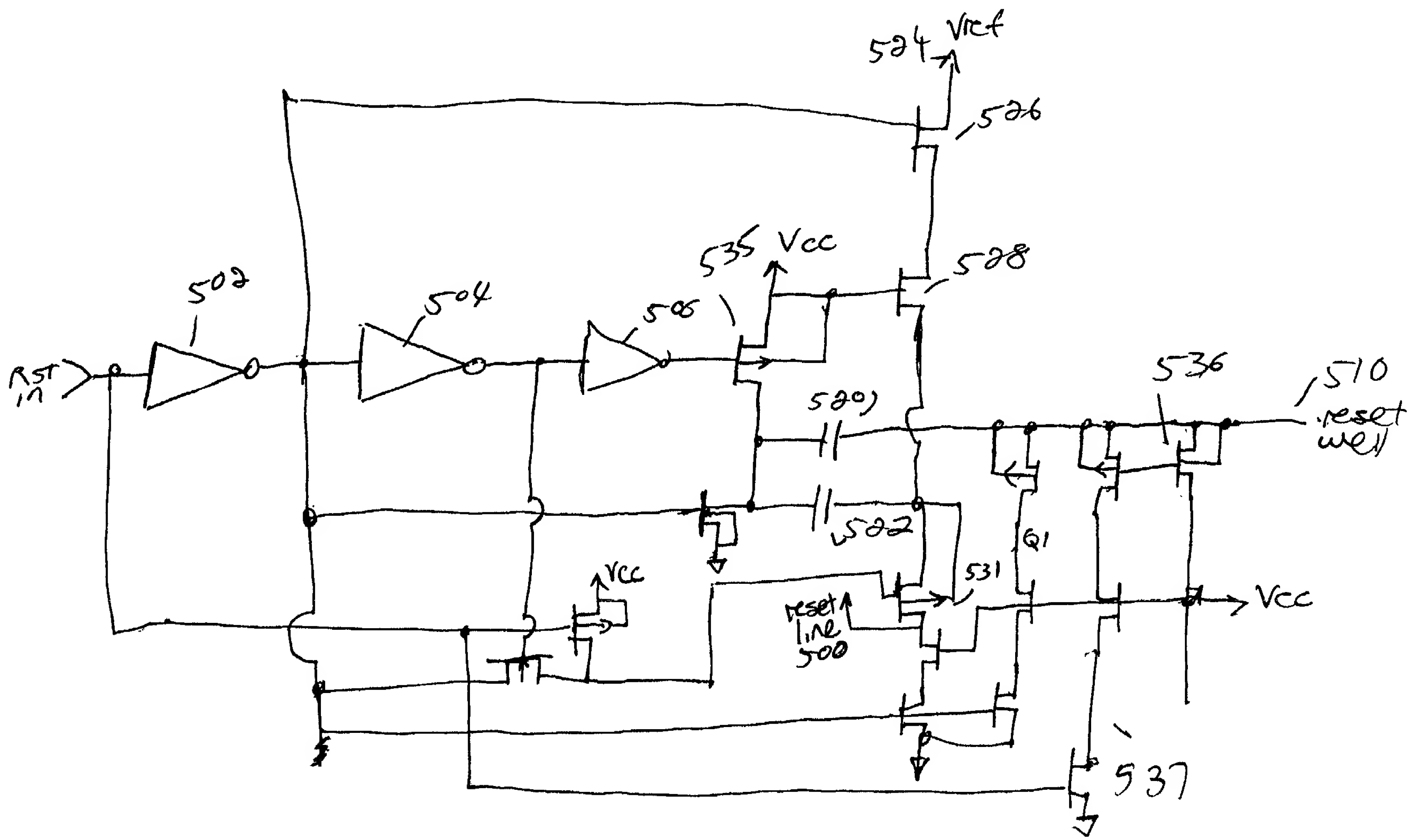

FIG 5

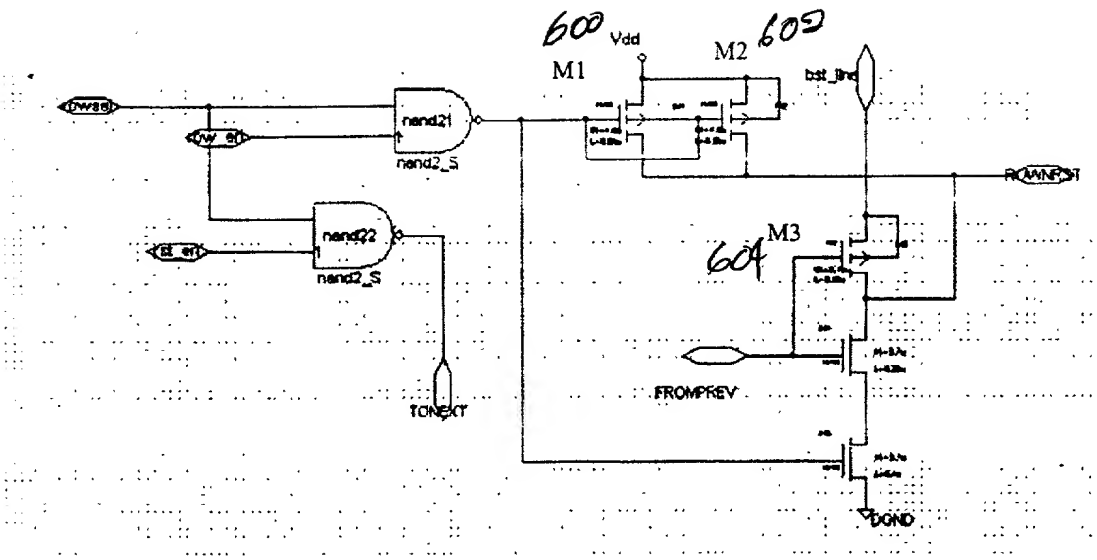

Figure 6 Current used row driver for shared ROW and boosting RST

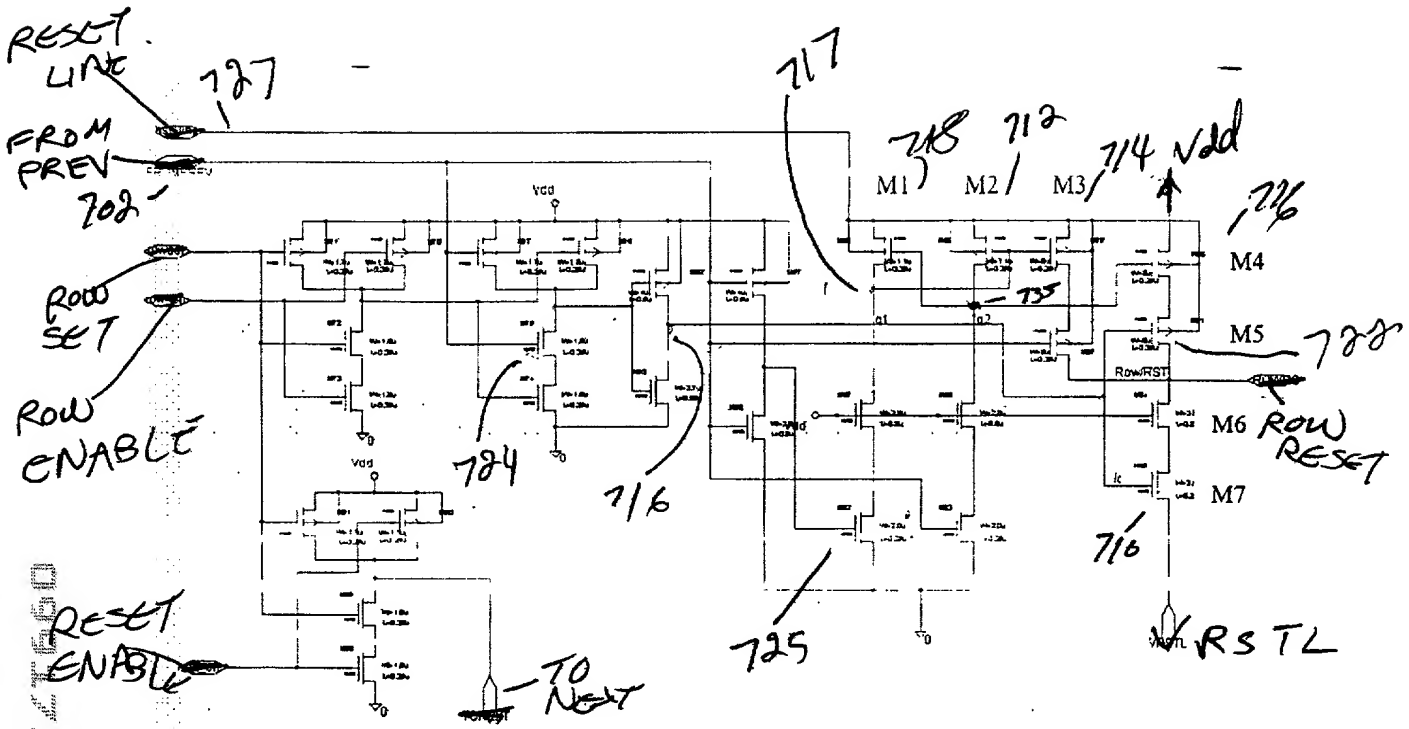

Figure 7. New row driver for shared ROW and boosting RST

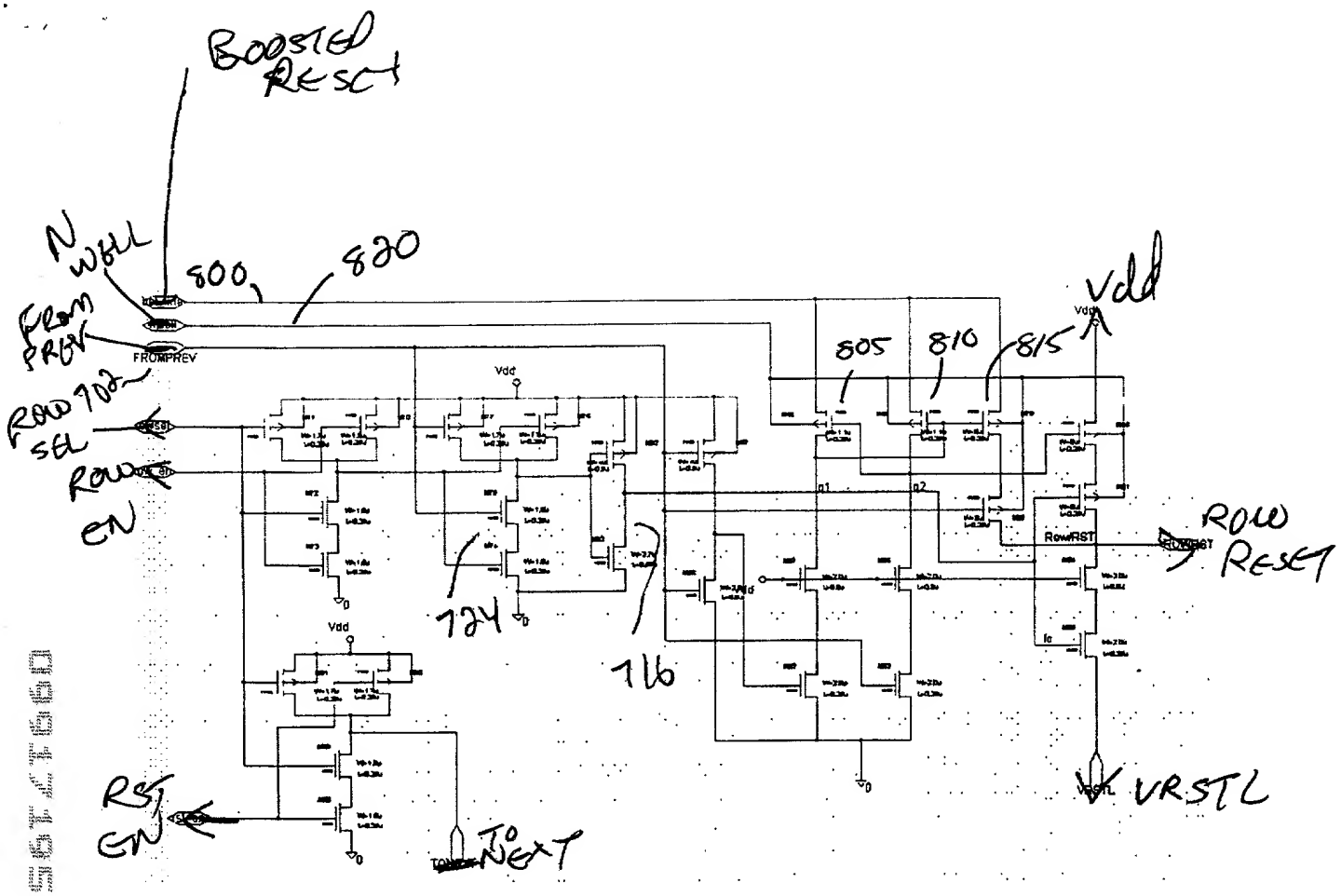

Figure 8. New row driver with separate boosting for RST and N-well

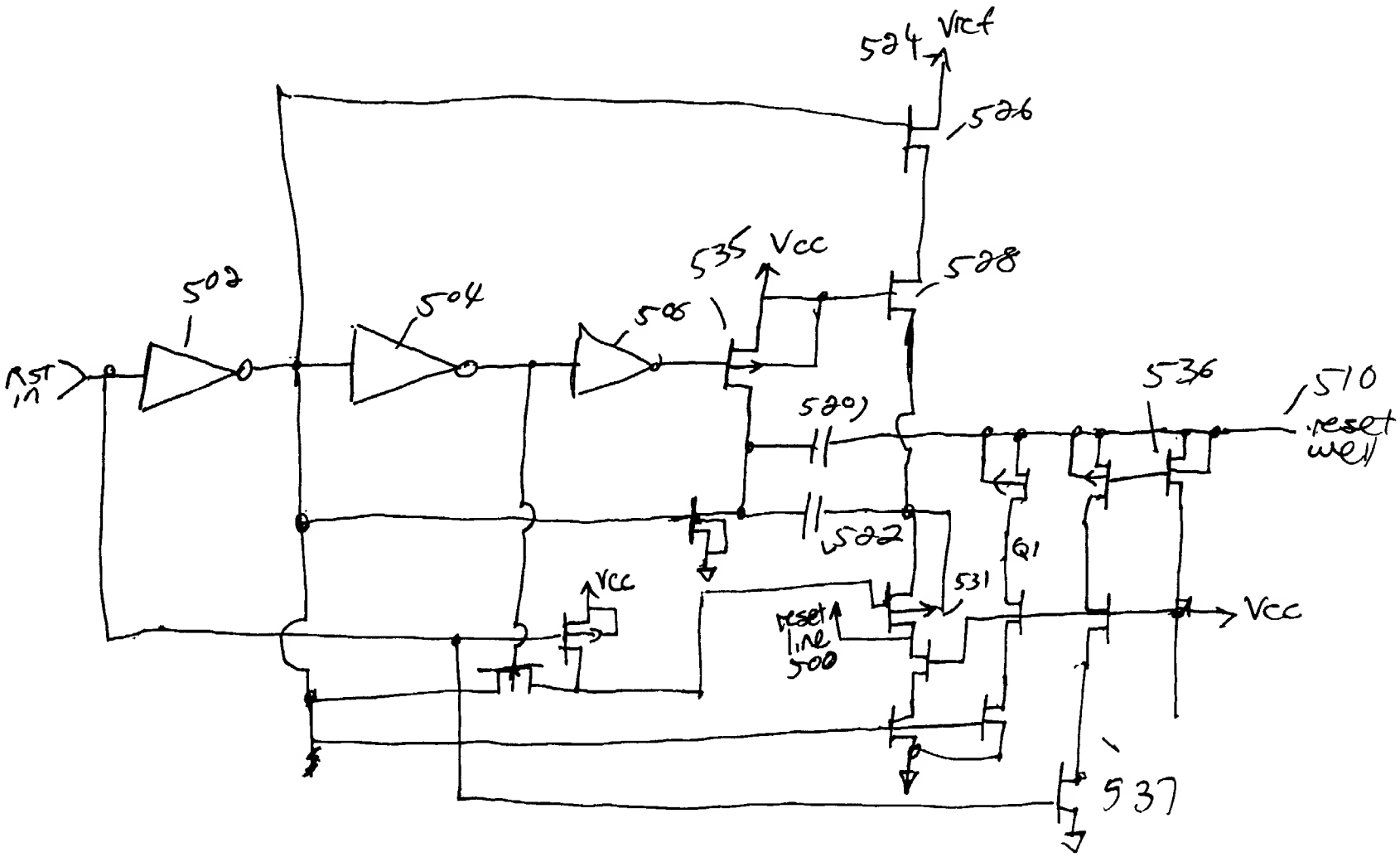

FIG 5